THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 15

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte HOWARD T. OLNOWICH,
DONALD G. GRICE AND ARTHUR R. WILLIAMS

_____

Appeal No. 96-0546
Application 07/947,010[1]

_____

ON BRIEF

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Before HAIRSTON, KRASS, and JERRY SMITH, Administrative Patent Judges.

HAIRSTON, Administrative Patent Judge.

_____

[1] Application for patent filed September 17, 1992.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 14 through 22. In view of appellants' withdrawal of the appeal of claims 17 and 19[2] (Brief, page 1), claims 14 through 16, 18 and 20 through 22 remain before us on appeal.

The disclosed invention relates to a bufferless switching network.

Claim 14 is illustrative of the claimed invention, and it reads as follows:

14. A bufferless switching apparatus comprising:

a plurality of switch inputs and a plurality of switch outputs;

connection means for establishing a requested communication path between any one of the switch inputs and any one of the switch outputs in response to a connection request included in a data message received at said any one of the switch inputs, said communication path for transmitting the data message received at said any one of the switch inputs to said any one of the switch outputs;

said connection means including asynchronous connection means for establishing asynchronously a plurality of simultaneously active requested communication paths between a

[2] The examiner's contentions (Answer, page 6) to the contrary notwithstanding, the withdrawal of claim 17 is not an admission by appellants that the claim "is properly rejected by the prior art of record."

plurality of switch inputs and a plurality of switch outputs in response to a plurality of connection requests each included in one of a plurality of data messages received separately or simultaneously at said plurality of switch inputs, said simultaneously active communication paths for transmitting simultaneously said plurality of data messages to said plurality of switch outputs;

said requested communication path and said simultaneously active requested communication paths each comprising a plurality of data paths for transmitting the data message, and a plurality of control paths, one of the control paths for transmitting a clock signal in parallel with the data message, a first pulse of the clock signal triggering the transmission of data message bits; and

a clock regeneration circuit at each switch input for receiving the data message and the clock signal and for transmitting a realigned data message and clock signal to said any one of the switch outputs, the clock regeneration circuit including delay means for adjusting a pulse width of the clock signal thereby aligning the clock signal and the data message bits for minimizing skew and pulse distortion between the clock signal and the data message bits.

The references relied on by the examiner are:

Upp	4,914,429	Apr. 3, 1990
Newman	4,965,788	Oct. 23, 1990
Todd	5,072,442	Dec. 10, 1991
Buhrke et al. (Buhrke)	5,231,631	July 27, 1993 (effective filing date Aug. 15, 1989)
Traw et al. (Traw)	5,274,768	Dec. 28, 1993 (filing date May 28, 1991)

Claims 14 through 16, 18 and 20 through 22 stand rejected under 35 U.S.C. § 103 as being unpatentable over Upp in view of Newman.

Claims 18 and 20 through 22 stand rejected under 35 U.S.C. § 103 as being unpatentable over Upp in view of Newman and either Todd, Traw or Buhrke.

Reference is made to the brief and the answer for the respective positions of the appellants and the examiner.

OPINION

We have carefully considered the entire record before us, and we will reverse the obviousness rejection of claims 14 through 16, 18 and 20 through 22.

Appellants and the examiner both agree (Brief, page 4, and Answer, page 5) that the clock regenerators 40a through 40p of Upp are located at the output ports as opposed to the input ports as required by claims 14 through 16, 18 and 20 through 22 on appeal. According to the examiner (Answer, page 5), "[i]t would have been obvious to one of ordinary skill in the art at the time of Appellant's [sic, Appellants'] invention to place the clock regenerators of Upp at the input port of the switching network, since it has been held that

rearranging parts of an invention involves only routine skill in the art." In the absence of evidence in the record that the circuit disclosed by Upp will still operate as intended with the modification suggested by the examiner, we agree with appellants' argument (Brief, pages 4 and 7) that Upp and Newman neither teach nor would they have suggested to the skilled artisan clock regenerators at an input. The additional references to Todd, Traw and Buhrke were cited by the examiner (Final rejection, paragraphs 19 and 20) for their teachings concerning nodes. Neither of these references cures the noted shortcoming in the teachings of Upp and Newman. Thus, the obviousness rejection of claims 14 through 16, 18 and 20 through 22 is reversed.

DECISION

The decision of the examiner rejecting claims 14 through 16, 18 and 20 through 22 under 35 U.S.C. § 103 is reversed.

REVERSED

KENNETH W. HAIRSTON Administrative Patent Judge	)	
ERROL A. KRASS Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
JERRY SMITH Administrative Patent Judge	)	

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